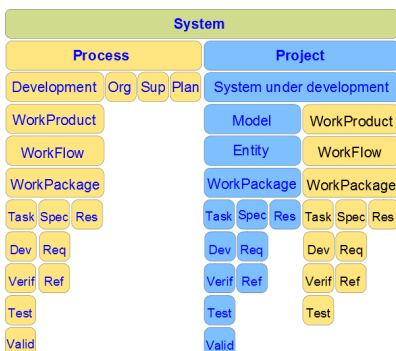


# From Deep Space to Deep Sea

## Trustworthy Embedded Systems Engineering

### Unique Open Technology Licensing offer from Altreonic for Certifiable Trustworthy Software and Systems

Altreonic offers advanced embedded systems technology under a unique risk-free **Open Technology License**. The licensee receives all supporting design documents, formal models, source code, test suites, etc. and the right to rebrand the software whereby all certification and business risks are seriously reduced. Free yourself from legacy COTS and open source limitations. Two technologies are offered: the formally developed, network-centric **VirtuosoNext™ Designer** and the internet based **GoedelWorks™** portal for supporting certifiable engineering projects. Soon to be integrated. Complemented with engineering services.



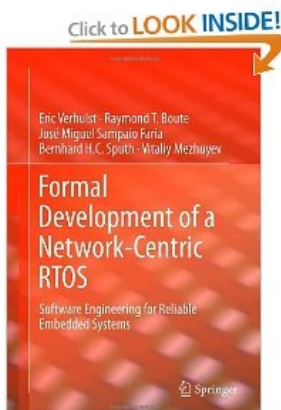
**GoedelWorks™** reflects our global “Correct by Construction” approach, covering from early requirements capturing till the last line of source code and hardware component.

Based on a formalised and clean meta-model, it allows describing any (engineering) process and support users executing it. Out-of-the-box support for ASIL centered IEC-61508, ISO-26262, ISO-13849, ISO-25119, ISO-15998 and IEC-62061, CMMI and automotive SPICE process flow. Integrate your own specific process flows for pre-certification support during the development of the system.

Implements the core concepts of any engineering standard: full traceability and configuration management.

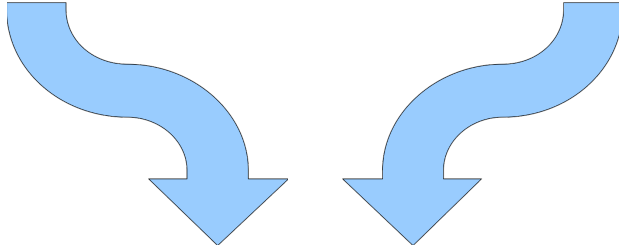
**VirtuosoNext™ Designer** breaks new grounds in the field of Real-Time Operating Systems. Formally designed and verified it is a 4<sup>th</sup> generation of the Virtuoso RTOS. Conceptually a scalable communication layer to support heterogeneous multi-processor systems in a transparent way, it runs equally well on a single processor. In protected mode it offers fine grain space and time partitioning.

It runs on small microcontrollers, many-core chips with little memory, parallel DSPs as well widely distributed systems and supports FPGAs. Unique support for distributed priority inheritance. Scalable, yet only requiring about 5 to 30 KB/node. Code is generated from a visual modeling environment. Full qualification package available.

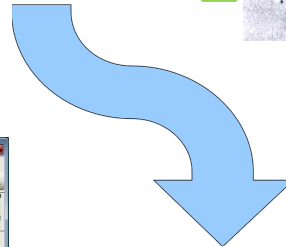
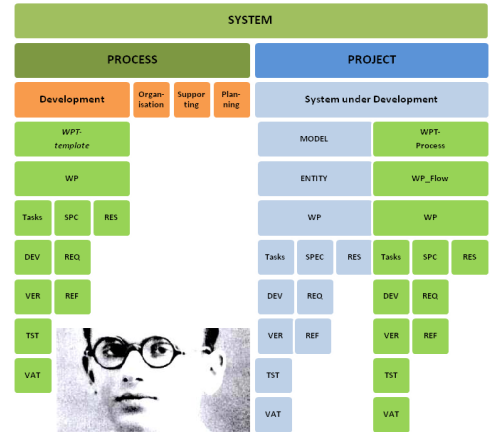


Customer specific  
Engineering  
Application Development

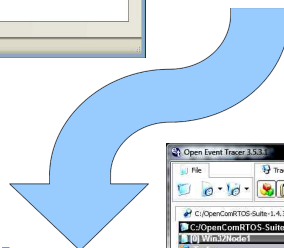
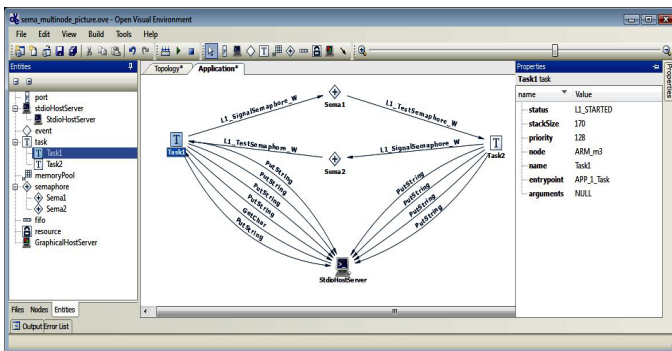
Correct by Construction  
Traceability for Qualification  
and Certification



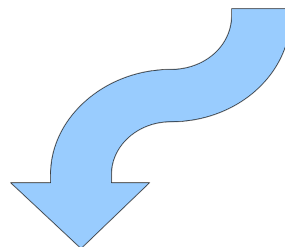
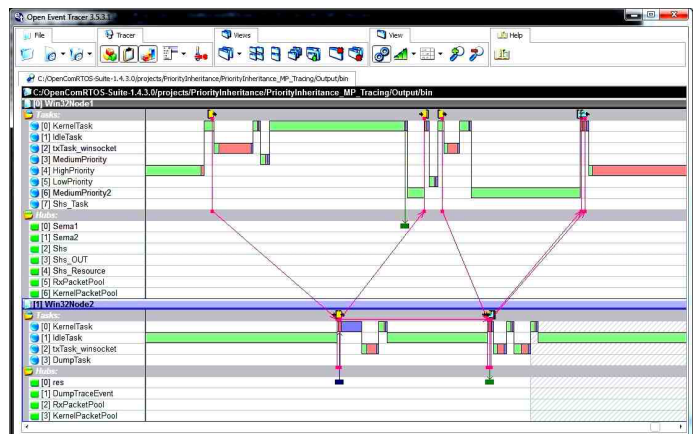
**GoedelWorks™**



**Visual  
Designer™**



**VirtuosoNext™  
OpenComRTOS™**



**Unified Systems Engineering**

for

**Trustworthy Systems**

